UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/662,480 | 09/16/2003 | Wataru Taki | 1248-0668P | 9630 |

2292 7590 06/13/2006

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

| EXAMINER | |
|---|---|
| LE, LANA N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2618 | |

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/662,480 | TAKI, WATARU | |
| | Examiner | Art Unit | |
| | Lana N. Le | 2618 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 4/3/06

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-7, 13, 16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-7, 13, 16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama et al (US 6,272,312) in view of Kashiwagi (US 4,661,995).

Regarding claim 1, Kashiwagi discloses a frequency conversion circuit (fig. 1) which performs a frequency conversion (via 6, 7) of a high frequency input signal (input signal at terminal 1) (col 3, lines 30-67), comprising:

a variable frequency filter (9) for removing a high harmonic wave of a first stage local oscillation signal (LO signal from 8) (col 4, lines 25-39).

Takayama et al do not disclose a two stage frequency conversion. Kashiwagi disclose a two stage frequency conversion stage (12, 13; fig. 2) with filtering the LO signal via 22a, 22b (figs. 4, 2) (col 4, line 39 - col 5, line 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the one stage frequency conversion circuit with the two stage frequency conversion circuit of Kashiwagi in order to allow adjustment of the oscillators and filters of the different frequency stages to suppress intermodulation disturbances as suggested by Kashiwagi.

Regarding claim 2, Takayama et al and Kashiwagi disclose the frequency

conversion circuit (fig. 1) as set forth in claim 1, wherein Takayama et al disclose the circuit further comprising:

a first stage local oscillation circuit (8); and a mixer circuit (6, 7), wherein said variable frequency filter (9) is provided between said first stage local oscillation circuit (8) and said mixer circuit (6, 7) (col 3, lines 45-60).

Regarding claim 3, Takayama et al and Kashiwagi disclose the frequency conversion circuit as set forth in claim 1, wherein Takayama et al disclose said variable frequency filter is a low pass filter (col 4, lines 25-29).

Regarding claim 4, Takayama et al and Kashiwagi disclose the frequency conversion circuit as set forth in claim 1, wherein Takayama et al disclose said variable frequency filter is a band pass filter (col 4, lines 25-29).

Regarding claim 5, Takayama et al and Kashiwagi disclose the frequency conversion circuit as set forth in claim 1, wherein Takayama et al disclose an inherent control section for controlling frequency characteristic of said variable frequency filter in response to a change in frequency of the local oscillation signal (col 4, lines 29-39).

Regarding claim 6, Takayama et al and Kashiwagi disclose the frequency conversion circuit as set forth in claim 5, wherein Kashiwagi discloses said control section (103) controls the frequency characteristic of said variable frequency filter (22a, 22b) using a phase lock loop (fig. 4) (col 4, lines 39-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to control the variable filter using a PLL in order to lock to the desired frequency by synchronizing the variable

oscillator with the phase of a transmitted signal and the oscillator of the PLL receives in a specific receiving band as suggested by Kashiwagi (col 4, lines 39-58).

Regarding claim 13, Takayama et al disclose a tuner (fig. 1) (col 3, lines 20-29) comprising: a frequency conversion circuit (6, 7) which performs a one stage frequency conversion of a high frequency input signal (input signal at terminal 1) (col 3, lines 30-67), the frequency conversion circuit comprising:

a variable frequency filter (9) for removing a high harmonic wave of a first stage local oscillation signal (LO signal from 8) (col 4, lines 25-39).

Takayama et al do not disclose a two stage frequency conversion. Kashiwagi disclose a two stage frequency conversion stage (12, 13; fig. 2) with filtering the LO signal via 22a, 22b (figs. 4, 2) (col 4, line 39 - col 5, line 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the one stage frequency conversion circuit with the two stage frequency conversion circuit of Kashiwagi in order to allow adjustment of the oscillators and filters of the different frequency stages to suppress intermodulation disturbances as suggested by Kashiwagi.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama et al (US 6,272,312) in view of Kashiwagi (US 4,661,995) and further in view of Cruz et al (5,054,117).

Regarding claim 7, Takayama et al and Kashiwagi disclose the frequency conversion circuit as set forth in claim 5, wherein Takayama et al disclose a tuning voltage is supplied to the variable filter and the oscillator (col 4, lines 40-47). Cruz et al disclose a control section (42; fig. 1) controls the frequency characteristic of said

variable frequency filter by a voltage synthesizer method (col 2, line 66 – col 3, line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to control the filter using a voltage synthesizer method in order to establish the resonant frequency.

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takayama et al (US 6,272,312) in view of Kashiwagi (US 4,661,995) and further in view Mao et al (US 2002/0,108,119).

Regarding claim 16, Takayama et al disclose a tuner (fig. 1) (col 3, lines 20-29) which comprises: frequency conversion circuit (6, 7) which performs a one stage frequency conversion of a high frequency input signal (input signal at terminal 1) (col 3, lines 30-67), the frequency conversion circuit comprising:

a variable frequency filter (9) for removing a high harmonic wave of a first stage local oscillation signal (LO signal from 8) (col 4, lines 25-39). Takayama et al do not disclose a two stage frequency conversion. Kashiwagi disclose a two stage frequency conversion stage (12, 13; fig. 2) with filtering the LO signal via 22a, 22b (figs. 4, 2) (col 4, line 39 - col 5, line 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the one stage frequency conversion circuit with the two stage frequency conversion circuit of Kashiwagi in order to allow adjustment of the oscillators and filters of the different frequency stages to suppress intermodulation disturbances as suggested by Kashiwagi. Takayama et al and Kashiwagi do not disclose a CATV receiving set top box comprising the tuner.

Mao et al disclose a CATV receiving set top box comprising a tuner (para. 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the tuner of Takayama et al and Kashiwagi within a CATV receiving set top box in order to receive both IP over MPEG internet data and MPEG encoded digital video preferred by the user using a single tuner as suggested Mao et al.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lana Le

6-06-06

LANA LE
PRIMARY EXAMINER